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DECEMBER
MAY 29 2002

MAY 29 2003

Prior Group Art Unit: 2814

Prior Examiner: WEISS

Commissioner for Patents
Washington, D.C. 20231

April 3, 2002

Transmitted herewith is an Amendment in the above-identified application.

* Small Entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.

A verified statement to establish Small Entity status under 37 CFR 1.9 and 1.27 is enclosed.

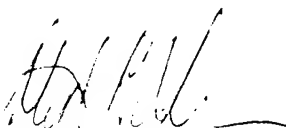
The fee has been calculated as shown below:

	CLAIMS AS AMENDED						
	Claims Remaining After Amendment	Highest Number Previously Paid For		Present Extra	Small Entity	Large Entity	Additional Fee
Total Claims	108	37	=	71	X \$9	X \$18	\$1,278.00
Independent Claims	10	3	=	7	X \$42	X \$84	588.00
## First Presentation of Multiple Dependent Claims					\$140	280	
TOTAL FEES ENCLOSED:							\$1,866.00

X Enclosed please find our check in the amount of **\$1,866.00** for the additional claims fee in connection with this amendment. The Commissioner is hereby authorized to charge payment for any additional fees associated with this communication or credit any overpayment to Deposit Account No. 01-2340. Two duplicates of this sheet are attached.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: IKEMASU et al.

Serial Number: 10/050,169

Filed: January 18, 2002

Prior Group Art Unit: 2814

For: HIGHLY INTEGRATED AND RELIABLE DRAM
AND ITS MANUFACTURE

Prior Examiner: WEISS

SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

April 3, 2002

Sir:

Further to the Preliminary Amendment filed on February 27, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please add new claims 38-108 as follows:

38. A semiconductor memory device comprising:
- a semiconductor substrate;
 - a memory cell transistor having impurity doped regions and a gate electrode;
 - an insulator laminate formed over said semiconductor substrate, and including a lower part covering said memory cell transistor and an upper part formed over said lower part;
 - a first contact hole, formed through said lower part of said insulator laminate, exposing one of said impurity doped regions;
 - a first conductor filled in said first contact hole and electrically connected to one of said